Post-OPC verification using a full-chip Pattern-Based simulation verification method

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ABSTRACT

In this paper, we evaluated and investigated techniques for performing fast full-chip post-OPC verification using a commercial product platform. A number of databases from several technology nodes, i.e. 0.13um, 0.11um and 90nm are used in the investigation. Although it has proven that for most cases, our OPC technology is robust in general, due to the variety of tape-outs with complicated design styles and technologies, it is difficult to develop a "complete or bullet-proof" OPC algorithm that would cover every possible layout patterns.

In the evaluation, among dozens of databases, some OPC databases were found errors by Model-based post-OPC checking, which could cost significantly in manufacturing – reticle, wafer process, and more importantly the production delay. From such a full-chip OPC database verification, we have learned that optimizing OPC models and recipes on a limited set of test chip designs may not provide sufficient coverage across the range of designs to be produced in the process. And, fatal errors (such as pinch or bridge) or poor CD distribution and process-sensitive patterns may still occur. As a result, more than one reticle tape-out cycle is not uncommon to prove models and recipes that approach the center of process for a range of designs. So, we will describe a full-chip pattern-based simulation verification flow serves both OPC model and recipe development as well as post OPC verification after production release of the OPC. Lastly, we will discuss the differentiation of the new pattern-based and conventional edge-based verification tools and summarize the advantages of our new tool and methodology:

1. Accuracy: Superior inspection algorithms, down to 1nm accuracy with the new "pattern based" approach
2. High speed performance: Pattern-centric algorithms to give best full-chip inspection efficiency
3. Powerful analysis capability: Flexible error distribution, grouping, interactive viewing and hierarchical pattern extraction to narrow down to unique patterns/cells

KEYWORD: Optical Proximity Correction (OPC), RET, full-chip post OPC verification, DFM, pattern-based

1. INTRODUCTION

As IC design complexity keeps increasing dramatically, mask fabrication rules restrict the coverage of process proximity correction to a severe situation. Both designers and manufacturers have encountered with more and more patterning challenges that would never happen in the past when the process generation is scaling down to 90nm and beyond. For example, DRC is no longer satisfying and sufficient with the real patterning rules. There are risks appeared more than usual if we still keep following with the past experience. Also, the space of correction has more constraint and limit in manufacturing. All of these would lead to serious impacts on the marginality of process windows, cost of process development, and most important, delay of product delivery. Because no customer and foundry can risk to ignore manufacturing impact on design, an approach to provide extremely fast, accurate verification and manufacturability optimization for RET/OPC --- a full-chip, model-based post-OPC verification solution, is becoming one of the most important key to secure the whole tape-out process.

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Down to the 90nm node and beyond, many patterning problems would not be caught and feedback until the layout is printed on the silicon. And traditional post-OPC checking, such as post-OPC MRC or XOR check, would not be capable of catching real and fatal problems. And by applying this solution, we can break down the only one feedback link and build up more shortcuts to quickly respond for any potential risk. (Figure.1)

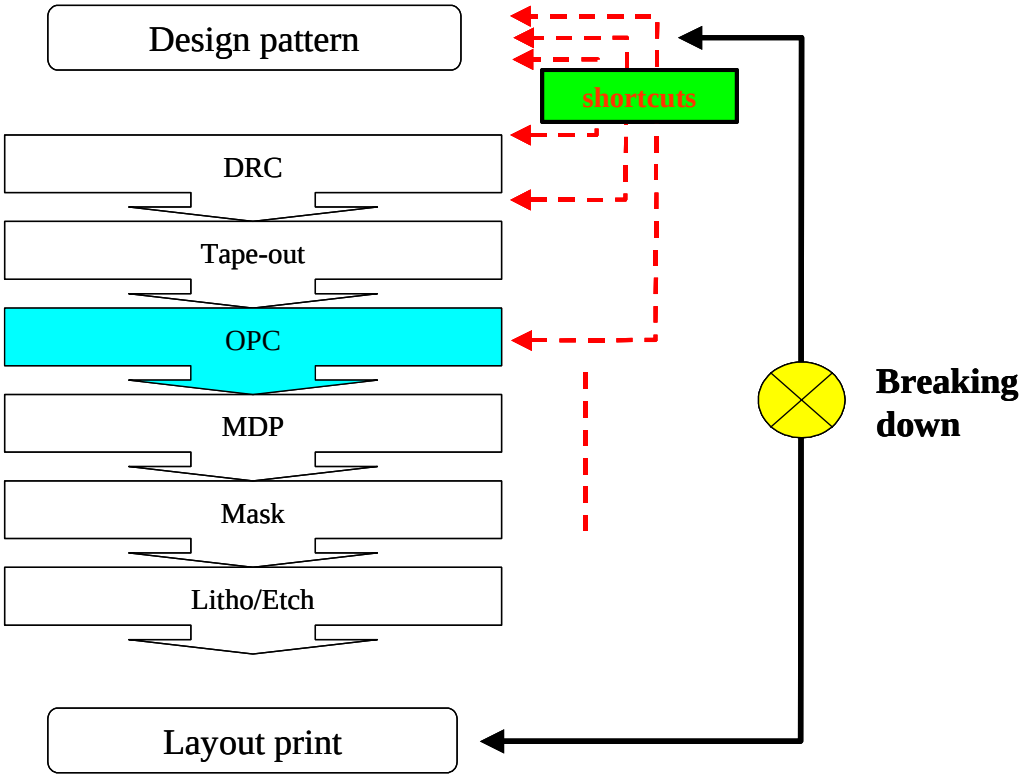

Figure.1: pattern transferring frame

The full-chip, model-based post-OPC verification tool applied in this paper is not only highly efficient, reliable and accurate, but also capable with all-around check items such as bridging, breaking, line-end or slot-end pullback, gate length CD uniformity, CT or VIA enclosure, contrast and MEEF, etc. All of them could cover powerfully about all RET/OPC concerns. Therefore, most of potentially fatal patterning failures could be captured and identified that which category those risks may belong to (Figure.2). Engineers can be warned much earlier before wafer is printed or even mask data is taped out. Then we can make judgment right more easily and fix the issues right on time. Finally, we can achieve to minimize the risk, save the cycle time, cost and of course, the yield.

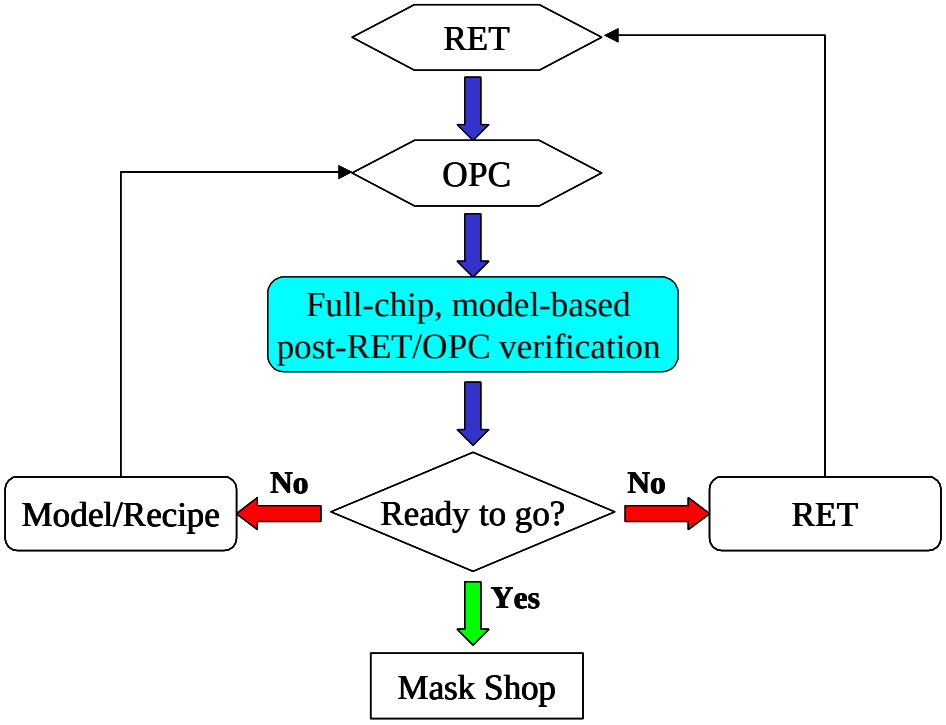

Figure.2: Efficient feedback loop of full-chip, model-based post-RET/OPC verification

2. THE NEW PLATFORM

The advanced technology enables smaller feature size and more complex design, which in turn, creates exponentially larger OPC data size. How to achieve high accuracy and at the same time, high full-chip performance becomes the challenge for the new generation of tools. Hot-spot output numbers are also getting larger on the scale of ten of thousands, even millions. How to efficient analyze hot-spot is also directly impacting the productivity and practicality of the tools.

Total inspection accuracy has two folds. Model accuracy is paramount and most obvious. However, the methodology for the building models is still ad hoc today. Model accuracy varies significantly from company to company, even using the same tool. The most common problem is insufficient data coverage, and data collection noise. A solid system approach must be implemented along with each tool. The lesser discussed portion of accuracy is coming from the full-chip simulation accuracy. Two issues are fundamentally critical. First, simulation steps (or inspection steps), also known as segmentations (fragmentations), need to be fine enough to catch fast changing OPC errors. For 90nm and below, 1nm step is not overly conservative.

Therefore, intensive computation is required when using conventional approach. Even with distributed computing, which is using large number of CPUs in parallel, such a algorithms will soon hit a limit as database size increases exponentially. Intelligent computation reduction has to be incorporated, and the algorithms have to take advantage of design database characteristics. Secondly, inspection coverage needs to be complete. For instance, the bridging inspection can check line to line, line to corner, and corner to corner, just to list a few; even an average design will have more complicated bridging conditions. Therefore, the inspection algorithms can be complicated and run time can be tedious. Several existing tools are prohibitive to use for large advanced designs for full-chip verification due to the limitations mentioned above.

NanoScope-PRV has a brand new, pattern-based engine, which treat polygon as patterns in comparison to edges for full-chip simulation; and it fundamentally improve the dilemma – accuracy vs. performance. While keeping simulation integrity, simulation is done at every nanometer to cover fast transition patterns, which can be missed by traditional methodology. In order to bring the full-chip performance to the next level, a patent pending algorithm is used to take advantage of pattern layout and design configurations. Multi-threading and distributed computing are also incorporated to speed up the inspection, and at the same time, to leverage existing networked hardware, and reduce overall system cost.

NanoScope has a set of utilities that provides cross-viewing between errors and GDS. It has built-in high performance pattern searching and matching algorithms, which can conveniently handle large error report, and sort ten of thousands, even millions of errors down to a small, manageable set of unique problems quickly and provide meaningful correction guidelines for OPC models, OPC recipes, as well as design change.

3. APPLICATION FLOW

NanoScope-PRV, specially designed for the new technologies is needed to extend the lifetime of current design style and fabrication process, it is powerful pre-masking layout verification software for yield enhancement.

This user-friendly platform can not only predict how the design will be printed on silicon by accurately simulating fabrication process conditions that affect pattern printing, and also tell us whether the design has potential downstream defects during fabrication process. It pinpoints the locations of potential real pattern defects in our layout design, and guides both of designers and manufacturers to correct the problems, which could severely affect the chip yield, before tape-out and making photo masks.

The potential defects it detects mainly belong to POLY end-cap, gate length shorting, gate length non-uniformity, open circuits, short circuits, via and metal overlap, layer misalignment, OPC anomaly, missing hammer heads, line bias, missing serifs, missing scattering bar, minimum spacing, none 45 degree lines, and cell or pattern mismatching.

At sub-wavelength lithography, the wall that traditional exists between design and manufacturing is disappearing. We need to address manufacturing issues at early stage to ensure customer's chip time-to-market and reduce total manufacturing cost. This post-OPC verification tool using a full-chip, pattern-based simulation verification method provides a mission-critical solution in the new era of chip design and manufacturing.

The verification approach in this paper (Figure.3) relies on silicon patterning process models. These models are characterized using photolithography system parameters, which include optical and photo resist parameters, and even etching parameters. The model would fit some critical photo-related varieties of phenomena (Figure.4 and Figure.5) such as through-pitch proximity effect, linearity, T-junction and head-to-head shorting based on the enormous database of wafer-level collection.

Here comes Figure. 3-5:

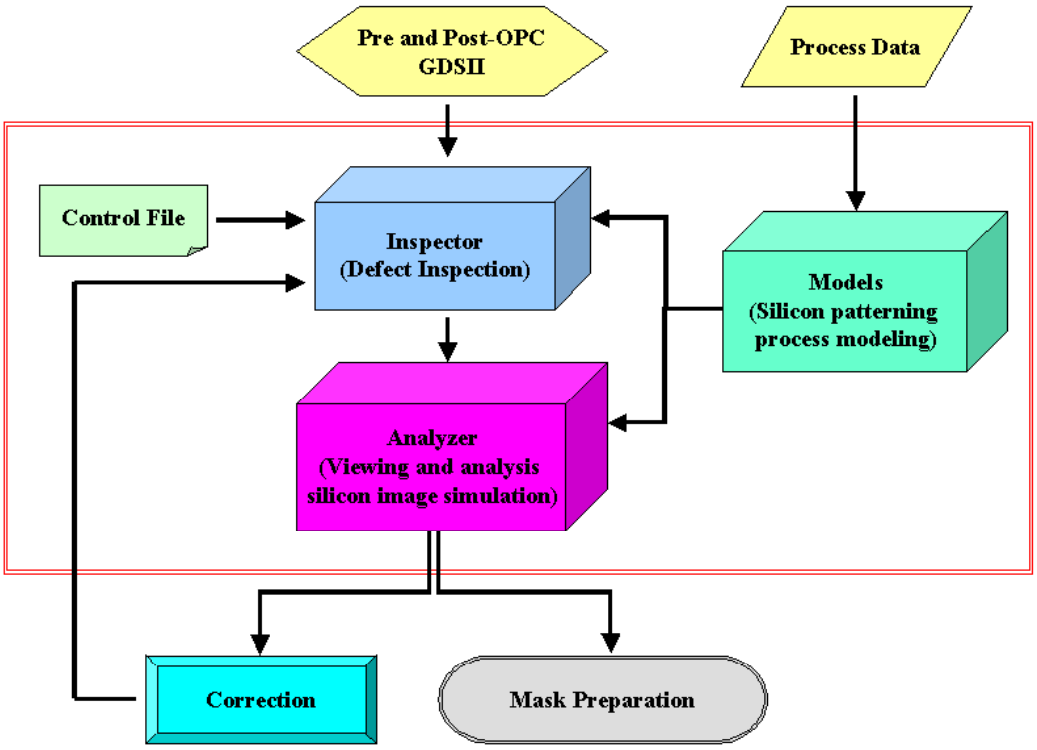

Figure.3: full-chip, pattern-based simulation verification application flow chart

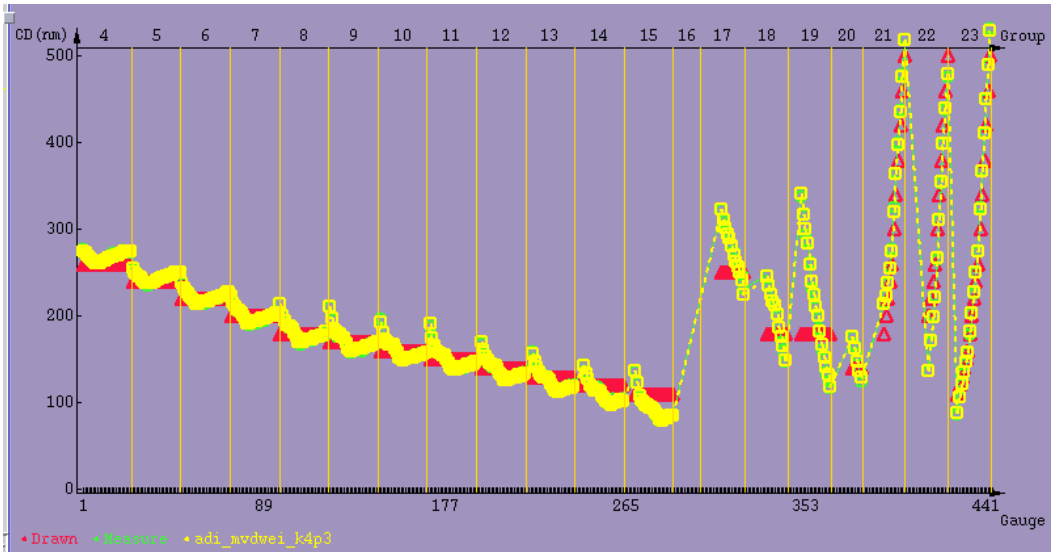

Figure.4: groups of photo-related phenomena

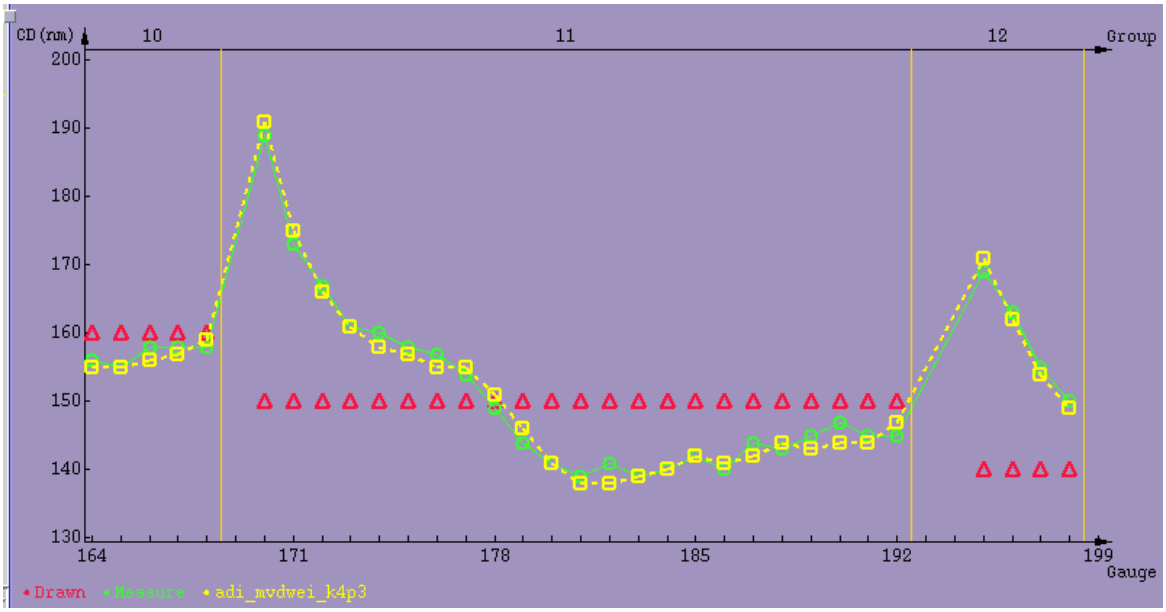

Figure.5: one of critical through-pitch proximity fitting curve

After confirming of model's fitting errors and convergence is within acceptable and reasonable range (Figure.6a and Figure.6b), we go forward to perform the full-chip or designated region defect inspection.

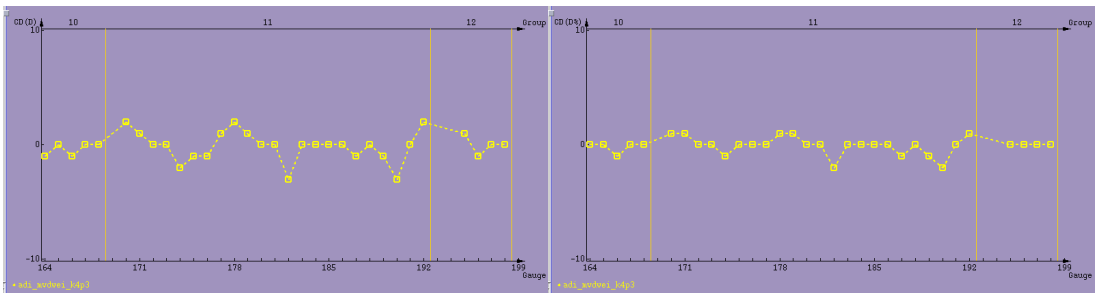

Figure.6a Figure.6b

Figure.6: (a) the model-to-wafer CD error fitness performance; (b) the percentage of model-to-wafer fitness error.

4. RESULTS AND DISCUSSION

NanoScope-PRV catches real production problems in the existing OPC operation flow, which can result significant manufacturing loss and production delay. Here we show are some real production cases of 0.13um logic (Figure.7) and 0.11um logic (Figure.8), which can all be detected since this powerful tool is being applied.

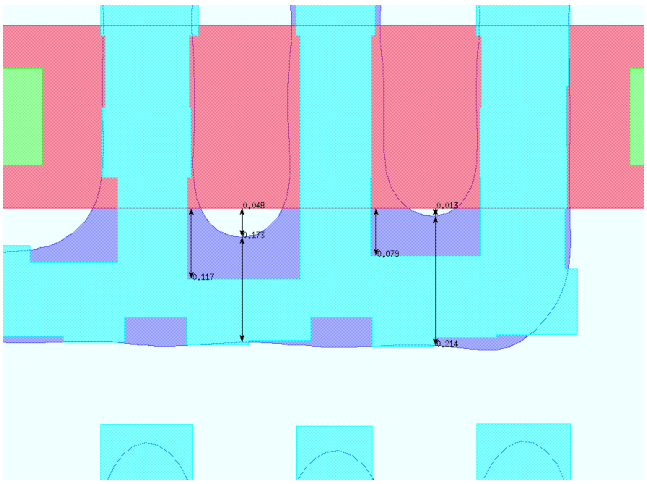

Figure.7a

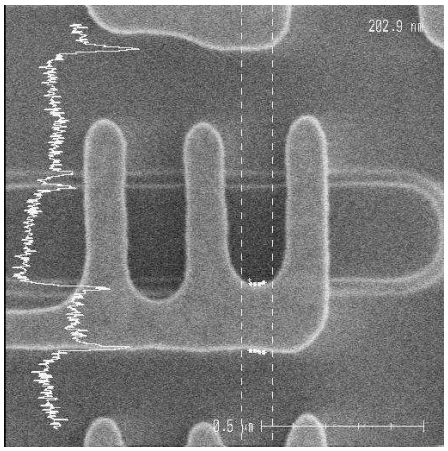

Figure.7b

Figure.7: (a) post-OPC correction and contour; (b) wafer-level confirmation (AEI).

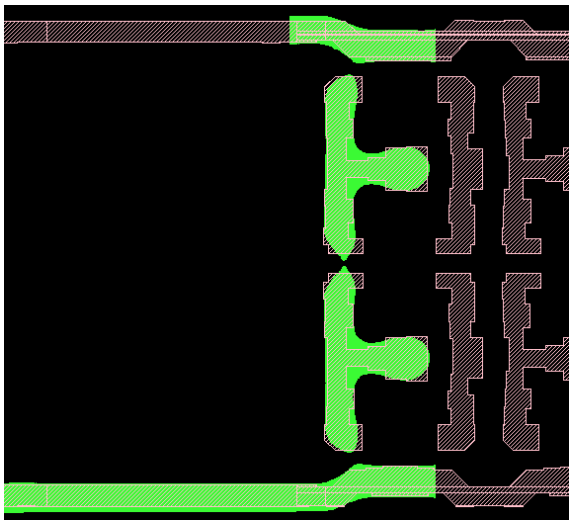

Figure.8a

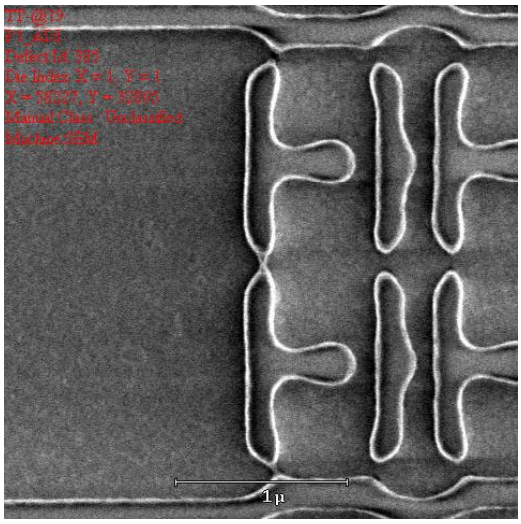

Figure.8b

Figure.8: (a) post-OPC correction and contour; (b) wafer-level confirmation (ADI).

5. CONCLUSION

New generation of technology requires new generation of tools to ensure the productivity driven moore's law. Based on the performance benchmark, NanoScope-PRV demonstrated a superior platform to address the new challenges in the mask synthesis flow. It not only simplifies our current verification flow, most importantly, it gives the confidence to the OPC process before making mask. Several systematic errors are caught by the tool in the production runs. Significant cost-saving including shorten production cycle were clearly demonstrated. Full-chip process window inspection and correction are also recommended for future work.

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